PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P04 114 WO	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/DK2004/000643	International filing date *(day/month/year)* 22.09.2004	Priority date *(day/month/year)* 22.09.2003
International Patent Classification (IPC) or national classification and IPC H03M1/50		
Applicant TC ELECTRONIC A/S ET AL.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 6 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 5 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☒	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
07.07.2005	10.10.2005
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized Officer Beindorff, W Telephone No. +31 70 340-2273

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/DK2004/000643

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-43	as originally filed
Claims, Numbers	
1-53	received on 09.07.2005 with letter of 07.07.2005
Drawings, Sheets	
1/27-27/27	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/DK2004/000643

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-53
	No:	Claims	none
Inventive step (IS)	Yes:	Claims	1-53
	No:	Claims	none
Industrial applicability (IA)	Yes:	Claims	1-53
	No:	Claims	none

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V.

1 The following documents are referred to in this communication:

D1 : SABOURI F ET AL: "A HIGH-PERFORMANCE CALIBRATION-FREE CHARGE-BALANCING ANALOG-TO-DIGITAL CONVERTER" IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, IEEE INC. NEW YORK, US, vol. 45, no. 5, October 1996 (1996-10), pages 847-853, XP000631687 ISSN: 0018-9456

D2 : DE 101 28 942 A (METTLER TOLEDO GMBH GREIFENSEE) 2 January 2003 (2003-01-02)

2 **Independent claim 1**

2.1 Document D1 discloses (see figures 1-3 and page 847, col. 2, line 25, to page 848, col. 1, line 11) an A/D converter (fig. 1) comprising a [charge-balancing][1] modulator (fig. 1 and 2), said converter comprising [a] loop comprising at least one forward path (from V_i to V_o) and at least one feedback path (from V_o to V_i via R_1), wherein the at least one forward path comprises amplitude quantizing means (the opamp having V_{th} at its inverting input) combined with time quantizing means (the D-flipflops) and outputting at least one time and amplitude quantized signal (V_o).

2.2 From this, the subject-matter of independent claim 1 differs in that according to claim 1 the modulator is a self-oscillating modulator and the A/D converter comprises at least one self-oscillating loop.

2.3 The subject-matter of claim 1 is therefore novel (Article 33(2) PCT).

2.4 The problem to be solved by the present invention may therefore be regarded as how to improve the accuracy of the time quantizing in a given frequency band compared to what should be expected based on the known properties of an available time quantizer. (See page 2, lines 17-19, of the description.)

2.5 The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) for the following reasons:
The problem is not addressed by D1, neither does it provide any indication why the skilled person would have reasons to replace the charge-balancing modulator by a self-oscillating

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1 For a better readability of this description features which are not in common with the application but form part of the solution provided by D1 are inserted in square brackets among the features which are in common.

one.

3 **Independent claim 46**
The subject-matter of independent claim 46 corresponds in terms of method features to that of independent claim 1. Thus, for the same reasons as set out in section 2 above, claim 46 is considered to be novel and to involve an inventive step.

4 **Dependent claims**
Claims 2-45 and 47-53 are dependent on claims 1 and 46 respectively and as such also meet the requirements of the PCT with respect to novelty and inventive step.

5 **Further comments**

5.1 **Further documents cited in the international search report**
Document D2 also discloses an amplitude and time quantizing A/D converter comprising a charge-balancing modulator, but its time quantizer is external to the loop, whereas that of D1 is inside the loop. Also D2 however does neither address the problem nor provide any indication as to its solution.

5.2 **Further documents cited in the description**
The documents cited at page 16 of the description all describe self-oscillating modulators per se, without mentioning any application to an A/D converter.

5.3 **Related priority application PCT/DK03/00613**
For the case that both this and the priority application are prosecuted in any national or regional phase it is noted that their sets of claims partially overlap.

Re Item VII.

The following is noted with respect to the description and drawings:

1 The *incorporation by reference* of the prior art documents at pages 16 and 17 of the description does not meet the requirements of Art. 5 PCT, see the PCT Guidelines, section 4.26.

2 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in

D1 is not mentioned in the description, nor is this document identified therein.

3 The application does not meet the requirements of Rule 11.13(k) PCT as in both the description and drawings figure number 27 has been skipped.

4 The term "amplitude time quantizing means" at page 4, lines 11 and 14, of the description is not defined in any claim to which these claims refer, neither is it clear by itself. It should probably read "amplitude **and** time quantizing means".

Re Item VIII.

The following is noted with respect to clarity (Art. 6 PCT):

1 Some dependent claims appear to refer to previous claims in which (part of) their features have not yet been defined: the switch frequency of claims 20-21 is defined for the first time in claim 19 only and thus undefined when these claims are taken dependent on any of claims 1-18. Similarly, the switch frequency of claims 50-51 is defined for the first time in claim 49 only.

2 In claim 44 "... the decimator is be greater ..." should probably read "... the decimator is greater...".

05.07.07 Amended claims

Patent claims

1. A/D converter comprising a self-oscillating modulator, said converter comprising

at least one self-oscillating loop comprising
at least one forward path,
at least one feedback path,

wherein said at least one forward path comprises amplitude quantizing means combined with time quantizing means and outputting at least one time and amplitude quantized signal.

2. A/D converter comprising a self-oscillating modulator according to claim 1, wherein said time quantizing means is arranged within said self-oscillating loop.

3. A/D converter comprising a self-oscillating modulator according to claim 1 or 2, wherein said time quantizing means comprises a high-speed sampling means.

4. A/D converter comprising a self-oscillating modulator according to any of the claims 1-3,
wherein said time quantizing means comprises a high-speed one-bit sampler.

5. A/D converter comprising a self-oscillating modulator according to any of the claims 1-4,
wherein said time quantizing means comprises latch-based circuitry comprising at least one latch, preferably at least two cascaded latches.

6. A/D converter comprising a self-oscillating modulator according to any of the claims 1-5,
wherein said amplitude quantizing means and said time quantizing means comprises a multi-bit A/D converter and where said feedback path comprises at least one D/A converter adapted for converting said time quantized signal into an analogue signal.

7. A/D converter comprising a self-oscillating modulator according to any of the claims 1-6,
wherein down sampling means are connected to said time quantizing means.

8. A/D converter comprising a self-oscillating modulator according to any of the claims 1-7,
wherein said A/D converter comprises two or more self-oscillating loops (SOL).

9. A/D converter comprising a self-oscillating modulator according to any of the claims 1-8,

wherein said amplitude and time quantizing means comprises an analogue two-level self-oscillating pulse width modulator.

10. A/D converter comprising a self-oscillating modulator according to any of the claims 1-8,
wherein said amplitude and time quantizing means comprises a multi-level self-oscillating pulse width modulator.

11. A/D converter comprising a self-oscillating modulator according to any of the claims 1-10,
wherein said A/D converter is single-ended.

12. A/D converter comprising a self-oscillating modulator according to any of the claims 1-11,
wherein said A/D converter is differential.

13. A/D converter comprising a self-oscillating modulator according to any of the claims 1-12,
wherein said A/D converter comprises filtering means, said filtering means adapted for band pass filtering the time quantized signal.

14. A/D converter comprising a self-oscillating modulator according to any of the claims 1-13, wherein the error originating from at least one time quantizer included in the at least one self-oscillating loop of the converter is suppressed by an error transfer functions which, at low frequencies approximates the inverse of the open-loop transfer functions of said at least one self-oscillating loop.

15. A/D converter comprising a self-oscillating modulator according to any of the claims 1-14, wherein the error originating from at least one time quantizer included in the at least one self-oscillating loop of the converter is suppressed by an error transfer functions which, at high frequencies approximates 0 dB.

16. A/D converter comprising a self-oscillating modulator according to any of the claims 1-15,
wherein said amplitude quantizing means comprises a limiter.

17. A/D converter comprising a self-oscillating modulator according to any of the claims 1-16, wherein said amplitude quantizing means comprises a frequency compensated limiter.

18. A/D converter comprising a self-oscillating modulator according to any of the claims 1-17,
wherein a variable self-oscillating loop delay is applied.

19. A/D converter according to any of the claims 1-18,

wherein A/D converter switches with a switch frequency which is at least partly defined by the at least one self oscillating loop.

20. A/D converter according to any of the claims 1-19,
wherein the switch frequency is at least 200 kHz, preferably at least 300 kHz.

21. A/D converter according to any of the claims 1-20,
wherein said A/D converter comprises switch frequency control means.

22. A/D converter according to claim 21,
wherein said switch frequency control means comprises a variable delay in said at least one self oscillating loop.

23. A/D converter according to claims 21 or 22,
wherein said switch frequency control means comprises an additional periodic signal generator connected to the self oscillating loop.

24. A/D converter according to any of the claims 21-23,
wherein said switch frequency control means comprises an oscillator or a derivative of a clock frequency.

25. A/D converter according to any of the claims 1-24,
wherein said at least one forward path comprises a non-linearity.

26. A/D converter according to claim 25,
wherein said non-linearity comprises a limiter.

27. A/D converter according to claims 25 or 26,
wherein said non-linearity comprises a frequency compensated limiter.

28. A/D converter according to any of the claims 25-27,
wherein said non-linearity comprises a comparator.

29. A/D converter according to any of the claims 25-28,
wherein said non-linearity comprises a operational amplifier.

30. A/D converter according to any of the claims 25-29,
the phase contribution of hysteresis in the non-linearity of the self-oscillating loop is less than 90°, preferably less than 40° at the switch frequency.

31. A/D converter according to any of the claims 25-30,
the phase contribution of hysteresis in the non-linearity of the self-oscillating loop at the switch frequency is less than 20°, preferably less than 10°.

32. A/D converter according to any of the claims 1-31,
wherein said at least one forward path and said at least one feedback path forms at least one self-oscillating loop.

33. A/D converter according to any of the claims 1-32,
wherein said self-oscillating loop forms a pulse width modulator and wherein the modulation of an analog input signal fed to the at least one forward path is pulse width modulated at least partly by oscillations established in said at least one self-oscillating loop.

34. A/D converter according to any of the claims 1-33,
wherein said self-oscillating modulator comprises at least one analog input connected to said forward path and wherein the output of said forward path is connected to a digital output.

35. A/D converter according to any of the claims 1-34,
wherein a transfer functions H(s) is inserted in the forward path, thereby at least partly controlling the switch-frequency.

36. A/D converter according to claim 35,
wherein the order of said transfer functions is at least one.

37. A/D converter according to claims 35 or 36,
wherein the order of said transfer functions is at least two.

38. A/D converter according to any of the claims 35-37,
wherein the effective order of said transfer functions is at least one, preferably substantially two.

39. A/D converter according to any of the claims 1-38,
wherein said A/D converter comprises an audio A/D-converter.

40. A/D converter according to any of the claims 1-39,
wherein the clock frequency of the time quantizing means is at least 10 (ten) times greater than the switch frequency of said at least one self-oscillating loop, preferably at least 100 (hundred) times greater.

41. A/D converter according to any of the claims 1-40,
wherein said quantization in the time domain is performed within said at least one self-oscillating loop.

42. A/D converter according to any of the claims 1-41,
wherein said A/D further comprises at least one decimator communicating with the digital output.

43. A/D converter according to claim 42,
wherein said decimator comprises an anti aliasing filter having an impulse response which longer that period of the pulse width modulated signal, preferably at least longer than three times the period of the pulse width modulated signal.

44. A/D converter according to claims 42 or 43, wherein the stopband attenuation of the underlying antialiasing filter of the decimator is be greater than 60dB, preferably greater than 100dB.

45. A/D converter according to claim 44, wherein the stopband of the antialiasing filter is:

Stopband = $k \cdot f_{Sout} \pm BW$, where k = 1,2,3,.... until the Nyquist frequency is reached,

f_{Sout} is the output rate of the decimator and BW is the utility bandwidth, typically preferably at least 20 kHz

46. Method of pulse width modulating an analog input signal into a pulse width modulated digital signal, whereby said analog input signal is modulated into a pulse width modulated representation by means of at least one self-oscillating loop

said self-oscillating loop comprising
at least one forward path,
at least one feedback path,

wherein said at least one forward path comprises amplitude quantizing means combined with time quantizing means and outputting at least one time and amplitude quantized signal,

47. Method of pulse width modulating an analog input signal according to claim 46, wherein said analog signal comprises an audio or audio derived signal.

48. Method of pulse width modulating an analog input signal according to claim 46 or 47,
whereby the method comprises the steps of representing a pulse width modulated representation as an analogue signal and quantizing the pulse width modulation in the time-domain and whereby said pulse width modulated representation is obtained by means of at least one self-oscillating modulator comprising at least one self-oscillating loop.

49. Method of pulse width modulating an analog input signal according to any of the claims 46-48,
wherein A/D converter switches with a switch frequency which is at least partly defined by the at least one self oscillating loop.

50. Method of pulse width modulating an analog input signal according to any of the claims 46-49,wherein said switch frequency is at least approximately 100 kHz, preferably at least 200 kHz and most preferably at least 300 kHz.

51. Method of pulse width modulating an analog input signal according to any of the claims 46-50, wherein the clock frequency of the time quantizing means is at least 10 (ten) times greater than the switch frequency of said at least one self-oscillating loop, preferably at least 100 (hundred) times greater.

52. Method of pulse width modulating an analog input signal according to any of the claims 46-51, wherein said method is performed in an audio A/D converter.

53.Method according to any of the claims 46-52, whereby said method is applied in an A/D converter according to any of the claims 1-4.